IN THE SPECIFICATION:

Please amend paragraph **[0007]** as follows:

[0007] An alternative method of dicing is disclosed in U.S. Patent No. 6,136,668 to Tamaki et al. Using this ~~technique~~ technique, a metal ~~layer~~ layer, in the form of a grid extending over the ~~streets~~ streets, is formed over an active surface of a silicon wafer. The silicon wafer body is singulated, but for the presence of the metal layer, by etching therethrough (after back grinding to reduce the wafer thickness) from the back side to the metal layer. The dice are then separated by melting and fusing the metal layer along the streets using a laser. Since this method involves etching through the entire thickness of the wafer and requires the presence of the metal layer as well as enough separation from the integrated circuitry of each semiconductor die to avoid damage from the laser-fused metal, the required width of the streets remains significant. This method also requires the extra steps to form the metal layer.

Please amend paragraph **[0010]** as follows:

[0010] The wafer is then singulated along the streets from the active surface side thereof with a laser beam, which may be of lesser width than the trenches. Potential damage to the resulting dice may be limited by using a narrower laser beam to cut through the reduced thickness of the wafer along the trenches, ~~lessening the potential for thermal stress due to a reduction in the time and energy along the trenches,~~ lessening the potential for thermal stress due to a reduction in the time and energy required for singulation and increasing the distance from the integrated circuitry on the active surface near the periphery of the semiconductor dice. The required width of the streets on the active surface of the wafer may thus be reduced, making additional wafer area available for semiconductor die fabrication.

Please amend paragraph **[0032]** as follows:

[0032] When trenches 106 are formed by etching, any conventional process steps used to perform the etching, such as disposing a mask material on the back side or bottom surface 103 of the semiconductor wafer 100 followed by photopatterning thereof, applying an etchant and,

optionally, a stop and maintaining the etching conditions, including without limitation temperature, are encompassed by and within the scope of the present invention. Prior to the formation of the trenches 106, the thickness of the semiconductor wafer 100 may be reduced, for example, to about 100 to about 200 μm to shorten the etch time required to form the trenches 106. For example, the back side or bottom surface of semiconductor wafer 100 may be abrasively or chemically abrasively ~~backg round,~~ background, chemically mechanically polished (CMP), or chemically etched back, as known to those of ordinary skill in the art.

Please amend paragraph **[0034]** as follows:

[0034] The thickness of the semiconductor wafer 100 to be severed by the laser 110 in the finish cut may be varied as is desired for the particular application. It is currently preferred that the remaining thickness of wafer body 107 at the bottom of trenches 106 be at least equivalent to the depth of the active circuitry formed in the active areas 102 of semiconductor wafer 100. This allows the formation of trenches 106 to take place with fairly high dimensional tolerances for trench location while reducing the risk that the integrity of integrated circuitry in the active areas 102 is compromised by trench 106 formation. Since the integrated circuitry typically only forms a small percentage of the thickness of semiconductor wafer 100, trenches 106 may be formed such that their depth penetrates the majority of the wafer 100 thickness. For example, a trench 106 may have ~~a depth~~ a depth of about 60% to about 90% of the wafer 100 thickness, leaving only about 10% to about 40% of the wafer to be finish cut.

Please amend paragraph **[0036]** as follows:

[0036] Trenches 106 may also be formed by a first laser cut occurring on the back side or bottom ~~surface103~~ surface 103 of the semiconductor wafer 100. One nonlimiting example of an embodiment of such a process, in accordance with the present invention, is depicted in FIG 4. A semiconductor wafer 100 has active areas 102 and streets 104 disposed adjacent a top or active surface 101 thereof. Trenches 106A are formed in the bottom surface 103 by initial trenching cuts made by a laser beam 132 generated by lower laser 130. As with trenches 106, discussed

previously herein, trenches 106A are formed in the back side or bottom surface 103, along paths coincident with streets 104 along which singulation is to be effected by the final cuts of the semiconductor wafer 100. A grid pattern of trenches 106A is thus formed, corresponding to the grid pattern of streets 104 on the active or top surface 101.

Please amend paragraph **[0037]** as follows:

[0037] Trenches 106A may be cut by laser ablation of the semiconductor material of wafer body 107 (again, following optional wafer thinning by backgrind or etch back) to a depth roughly equivalent to, but slightly less than, the depth the integrated circuitry of active areas 102 is formed in the wafer 100. Since the integrated circuitry typically only forms a small percentage of the thickness of semiconductor wafer 100, trenches 106A may be cut such that their depth penetrates the majority of the wafer 100 thickness. For example, a trench 106A may have ~~a depth~~ a depth of about 60% to about 90% of the wafer 100 thickness, leaving only about 10% to about 40% of the wafer thickness to be finish cut. Of course, it will be appreciated that where appropriate, trenches 106A may be cut to other depths. For example, where fine focus, orientation and directional control of the lower laser 130 is possible, trench 106A may extend upwardly past the depth at which active areas 102 penetrate the wafer 100. However, in many instances the cost of such equipment and the time involved in effecting precision laser cuts renders the making of an initial, wider laser cut at a lower resolution more desirable.

Please amend paragraph **[0043]** as follows:

[0043] One possible arrangement for the first set of lasers A may be a bank of lasers comprising a plurality of lasers 200 fixed in a single row and spaced a predetermined distance apart, which distance, of course, may be adjusted for different die shapes and sizes. Where streets 104 of the wafer 100 are parallel, as is conventional, singulation may be accomplished by traversing the entire bank A of lasers 200 across a wafer 100 in a direction perpendicular to the row such that laser beams 202 thereof pass simultaneously through material of wafer body 107 along the streets 104. Where the streets form a conventional grid pattern across the

semiconductor wafer 100, the bank A of lasers 200 may be traversed across the wafer 100 along a first directional path (multiple times with each pass over wafer 100 preceded by an appropriate offsetting of the ganged lasers 200 in a direction parallel to the row if fewer lasers 200 are present than parallel streets 104 on semiconductor wafer 100). Subsequently, when cuts have been made along all parallel streets 104, the semiconductor wafer 100 may be rotated 90° using wafer holder or chuck 210 about a vertical axis perpendicular to the plane thereof (or the bank of lasers 200 rotationally moved 90° to traverse a second directional path perpendicular to the first) and then traversed across the semiconductor wafer 100 to make a second series of cuts, perpendicular to the first series. Of course, it will be appreciated that the semiconductor wafer 100 may be moved or translated relative to the bank of lasers 200 instead. Where necessary, individual lasers 200 may be turned off or the laser beams ~~thereof~~ 202 thereof may be redirected, to facilitate singulation.